WHAT IS CLAIMED IS:

1. A transistor, comprising:

a source and a drain disposed in a workpiece, the workpiece having a top surface, the source and drain being separated by a channel region, wherein the source and drain each comprise a dopant-bearing metal region disposed within the top surface of the workpiece, and a doped region disposed in the workpiece adjacent each dopant-bearing metal region;

a gate dielectric disposed over the channel region and a portion of the source and the drain; and

a gate disposed over the gate dielectric.

2. The transistor according to Claim 1, wherein the dopant-bearing metal regions comprise a thickness of about 200 Å or less.

3. The transistor according to Claim 2, wherein the dopant-bearing metal regions comprise TiB_2, ZrB_2, HfB_2, ZrP, TiP, $ZrSb_2$, $TiSb_2$, $HfSb_2$, or arsinides of Zr or Hf.

4. The transistor according to Claim 1, wherein the doped regions comprise a thickness of about 100 Å or less.

5. The transistor according to Claim 1, wherein the dopant-bearing metal regions and a dopant in the doped regions comprise B, P, As, or Sb.

6. The transistor according to Claim 1, wherein the source and the drain comprise a thickness of about 300 Å or less below the top surface of the workpiece.

7. The transistor according to Claim 1, wherein the gate dielectric comprises a high dielectric constant material, silicon dioxide (SiO_2), silicon nitride (Si_xN_y) or silicon oxynitride (SiON).

8. The transistor according to Claim 7, wherein the gate dielectric comprises HfO_2, $HfSiO_X$, Al_2O_3, ZrO_2, $ZrSiO_X$, Ta_2O_5, La_2O_3, SiO_2, Si_xN_y, SiON, or combinations thereof.

9. The transistor according to Claim 1, further comprising an interfacial dielectric disposed between the gate dielectric and the channel region of the workpiece.

10. The transistor according to Claim 9, wherein the interfacial dielectric comprises a thickness of about 7 Å or less.

11. The transistor according to Claim 1, wherein the gate and the gate dielectric comprise sidewalls, further comprising a first spacer disposed over the sidewalls of the gate and the gate dielectric.

12. The transistor according to Claim 11, wherein the first spacer comprises a width of about 20 Å to about 70 Å.

13. The transistor according to Claim 11, wherein the first spacer comprises sidewalls, further comprising a second spacer disposed abutting the sidewalls of the first spacer.

14. The transistor according to Claim 1, wherein the source and the drain each comprises a deep implantation region disposed beneath each doped region.

15. A semiconductor device comprising at least one transistor according to Claim 1.

16. The semiconductor device according to claim 15, wherein the at least one transistor comprises a PMOS transistor, an NMOS transistor, or both.

17. A transistor, comprising:

a source disposed in a workpiece, the workpiece having a top surface, wherein the source comprises a first dopant-bearing metal region disposed within the top surface of the workpiece and a first doped region disposed within the workpiece adjacent the first dopant-bearing metal region;

a drain disposed in the workpiece, the drain being separated from the source by a channel region, wherein the drain comprises a second dopant-bearing metal region disposed within the top surface of the workpiece and a second doped region disposed within the workpiece adjacent the second dopant-bearing metal region;

a gate dielectric disposed over the channel region and a portion of the source and the drain; and

a gate disposed over the gate dielectric.

18. The transistor according to Claim 17, wherein the dopant-bearing metal region comprises about 100 Å or less of TiB_2, ZrB_2, HfB_2, ZrP, TiP, $ZrSb_2$, $TiSb_2$, $HfSb_2$, or arsinides of Zr or Hf.

19. The transistor according to Claim 17, wherein the gate dielectric comprises HfO_2, $HfSiO_X$, Al_2O_3, ZrO_2, $ZrSiO_X$, Ta_2O_5, La_2O_3, SiO_2, Si_xN_y, SiON, or combinations thereof.

20. A method of fabricating a transistor, the method comprising:

providing a workpiece;

depositing a gate dielectric material over the workpiece;

depositing a gate material over the gate dielectric material;

patterning the gate material and the gate dielectric material to form a gate and a gate dielectric over a channel region of the workpiece;

forming a first recess in a source region of the workpiece and a second recess in a drain region of the workpiece, the source region and the drain region being proximate and separated by the channel region;

filling the first recess and the second recess with a dopant-bearing metal; and

annealing the workpiece to cause diffusion of a dopant of the dopant-bearing metal into the workpiece and form a doped region within the workpiece adjacent the dopant-bearing metal in the source region and the drain region.

21. The method according to Claim 20, wherein annealing the workpiece comprises a temperature of about 900 °C or less for about 1 hour or less.

22. The method according to Claim 20, wherein the gate dielectric comprises sidewalls, wherein filling the first recess and the second recess with the dopant-bearing metal comprises:

depositing the dopant-bearing metal over the first recess, the second recess, the gate, and the sidewalls of the gate dielectric; and

removing the dopant-bearing metal from over the gate and sidewalls of the gate dielectric, leaving the dopant-bearing metal in the first recess and the second recess.

23. The method according to Claim 20, wherein the gate and the gate dielectric comprise sidewalls, further comprising forming a first spacer on the sidewalls of the gate and the gate dielectric, before forming the first recess and the second recess.

24. The method according to Claim 23, wherein forming the first spacer comprises forming a spacer comprising a width of about 20 Å to about 70 Å.

25. The method according to Claim 23, further comprising implanting ions of a dopant into the source region and the drain region, after forming at least the first spacer, and annealing the workpiece to form deep implantation regions in the source region and the drain regions beneath the doped regions.

26. The method according to Claim 23, wherein the first spacer comprises sidewalls, further comprising forming a second spacer over the sidewalls of the first spacer, after annealing the workpiece.

27. The method according to Claim 26, further comprising implanting ions of a dopant into the source region and the drain region, after forming the second spacer, and annealing the workpiece to form deep implantation regions in the source region and the drain regions beneath the doped regions.

28. The method according to Claim 20, wherein forming the first recess and the second recess comprise forming recesses having a depth of about 200 Å or less.

29. The method according to Claim 28, wherein filling the first recess and the second recess with a dopant-bearing metal comprises filling the first recess and the second recess with TiB_2, ZrB_2, HfB_2, ZrP, TiP, $ZrSb_2$, $TiSb_2$, $HfSb_2$, or arsinides of Zr or Hf.

30. The method according to Claim 20, wherein forming the first recess and the second recess comprise a single patterning step.

31. The method according to Claim 20, wherein depositing the gate dielectric material comprises depositing HfO_2, $HfSiO_X$, Al_2O_3, ZrO_2, $ZrSiO_X$, Ta_2O_5, La_2O_3, SiO_2, Si_xN_y, SiON, or combinations thereof.